Raúl Taranco, Ph.D.

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Current Position

I am currently a postdoctoral researcher at the ARCO Lab, Universitat Politècnica de Catalunya (UPC), where I develop energy-efficient, high-performance hardware architectures for mobile vision systems. My research includes designing hardware accelerators, extending CPU microarchitectures, and leveraging hardware-software co-design techniques to significantly enhance performance and power efficiency in emerging applications such as robotics, autonomous driving, and augmented/virtual reality.

Interests

My future research interests include Computer Architecture, Hardware-Software Co-design, Machine Learning for Computer Architecture, Visual Computing Systems, Autonomous Systems, and Edge and Embedded AI.

Education

Ph.D. in Computer Architecture (Cum Laude) *2024*
Universitat Politècnica de Catalunya (UPC)
- **Thesis:** "Architectural Strategies to Enhance the Latency and Energy Efficiency of Mobile Continuous Visual Localization Systems"
- **Advisors:** Jose-Maria Arnau, Antonio González

M.S. in Computer Engineering and High Performance Computing *2019*
Universitat Politècnica de Catalunya (UPC)
- **Thesis:** "A Hardware Accelerator for ORB-SLAM"
- **Advisors:** Jose-Maria Arnau, Antonio González

B.S. in Computer Science, with Honors *2016*
Universidad de Cantabria (UC)
- **Thesis:** "Development and Evaluation of a Hardware-Friendly Encoder for HTM Systems"
- **Advisor:** Valentín Puente Varona

Experience

Postdoctoral Researcher *2024 – Present*
ARCO Lab, Universitat Politècnica de Catalunya (UPC)
Barcelona, Spain
- Conduct research on energy-efficient architectures for mobile vision and ray-tracing GPUs in collaboration with Prof. Antonio González and Prof. Juan Luis Aragón.
- Developed proposals for Marie Skłodowska-Curie Actions (MSCA) and national funding programs.

AI Scientific Advisor *2024 – Present*
Medidedalia
Barcelona, Spain
- Advise the company on the implementation of AI models for enhancing patient safety and optimizing medical claims processing.

Visiting Researcher *2023*
Harvard University, John A. Paulson School of Engineering and Applied Sciences
Boston, MA, USA
- Conducted research in robotics and autonomous driving under the guidance of Prof. Vijay Janapa Reddi.

Research Assistant *2019 – 2024*
ARCO Lab, Universitat Politècnica de Catalunya (UPC)
Barcelona, Spain
- Researched hardware architectures for mobile vision and AI accelerators with Prof. Antonio González and Dr. Jose-María Arnau.
- Evaluated computer vision workloads on cutting-edge architectures.

- Designed domain-specific accelerators, CPU vector extensions, and hardware-software co-designs for AR, robotics, and autonomous systems.

Teaching Assistant *2021 – 2023*
Universitat Politècnica de Catalunya (UPC)
Barcelona, Spain

Research Assistant *2016*
Universidad de Cantabria (UC)
Santander, Spain

- Investigated Hierarchical Temporal Memory (HTM) and Sparse Distributed Representations (SDRs).
- Designed a hardware-efficient scalar encoder for SDRs.

Publications

[1] **Raúl Taranco** and Antonio González. "Enabling Motion-Based Sampling for Energy-Efficient Machine Vision". In: *Under Review*. 2025.

[2] **Raúl Taranco**, José-María Arnau, and Antonio González. "IRIS: Unleashing ISP-Software Cooperation to Optimize the Machine Vision Pipeline". In: *Proceedings of the 31st International Symposium on High-Performance Computer Architecture (**HPCA'25**)*. Las Vegas, NV, USA: Association for Computing Machinery, 2025, Accepted for publication.

[3] **Raúl Taranco**, José-María Arnau, and Antonio González. "SLIDEX: A Novel Architecture for Sliding Window Processing". In: *Proceedings of the 38th ACM International Conference on Supercomputing (**ICS'24**)*. New York, NY, USA: Association for Computing Machinery, June 2024, pp. 312–323. URL: https://dl.acm.org/doi/10.1145/3650200.3656613.

[4] **Raúl Taranco**, José-María Arnau, and Antonio González. "δLTA: Decoupling Camera Sampling from Processing to Avoid Redundant Computations in the Vision Pipeline". In: *Proceedings of the 56th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO'23**)*. Toronto, Canada: Association for Computing Machinery, Dec. 2023, pp. 1029–1043. URL: https://dl.acm.org/doi/10.1145/3613424.3614261.

[5] **Raúl Taranco**, José-María Arnau, and Antonio González. "SLIDEX: Sliding Window Extension for Image Processing". In: *2023 32nd International Conference on Parallel Architectures and Compilation Techniques (**PACT'23**)*. Vienna, Austria, 2023, pp. 332–334. URL: https://ieeexplore.ieee.org/document/10364589?signout=success.

[6] **Raúl Taranco**, José-Maria Arnau, and Antonio González. "LOCATOR: Low-power ORB accelerator for autonomous cars". In: *Journal of Parallel and Distributed Computing (**JPDC**)* 174 (2023), pp. 32–45. URL: https://www.sciencedirect.com/science/article/pii/S0743731522002507.

[7] **Raúl Taranco**, José-Maria Arnau, and Antonio González. "Sliding Window Support for Image Processing in Autonomous Vehicles". In: *Workshop on Compute Platforms for Autonomous Vehicles (**CAV**), held in conjunction with 55th IEEE/ACM International Symposium on Microarchitecture (**MICRO'22**), Chicago (Illinois, USA)*. 2022. URL: https://sites.google.com/g.harvard.edu/cav-micro22/ (visited on 09/04/2022).

[8] **Raúl Taranco**, José-Maria Arnau, and Antonio González. "A low-power hardware accelerator for ORB feature extraction in self-driving cars". In: *2021 IEEE 33rd International Symposium on Computer Architecture and High Performance Computing (**SBAC-PAD'21**)*. IEEE. 2021, pp. 11–21.

Teaching

Advanced Processor Architecture *2025*
Universitat Politècnica de Catalunya (UPC)

- Seminars for MSc Computer Engineering students on processor microarchitecture, including topics on prefetching and branch prediction.

Computer Organization *2021 – 2023*
Universitat Politècnica de Catalunya (UPC)

- Delivered 90+ hours of lab sessions for BSc Computer Engineering students, covering instruction set architectures, pipelining, and memory hierarchies.

Awards and Recognitions

- **2025:** HiPEAC Paper Award
- **2024:** ICS Student Travel Grant
- **2023:** HiPEAC Paper Award
- **2019:** FPU Ph.D. Grant (Spanish MECD) for doctoral studies and teaching training
- **2017:** Bachelor's Degree Extraordinary Award (Top graduate distinction)
- **2016:** Spanish MECD Collaboration Grant, Computer Architecture Dept., Universidad de Cantabria

Research Projects

Domain-Specific Architectures for Energy-Efficient Computing Systems *2021 – Present*
- Researcher. Funded by the Spanish State Research Agency (MCIN/AEI), Grant PID2020-113172RB-I00.

CoCoUnit: An Energy-Efficient Processing Unit for Cognitive Computing *2019 – Present*
- Researcher. Funded by the European Research Council (ERC), Grant No. 833057.

Conferences and Training

Issues in Computer Architecture and Microarchitecture for Future Computing Machines *2019*
- Seminar by Prof. Yale Patt (University of Texas at Austin).

PUMPS + AI Summer School 2019 *2019*
- Organized by Barcelona Supercomputing (BSC) Center and UPC.

Languages

- **Spanish:** Native
- **English:** Fluent

Skills and Competences

- **Programming Languages & Frameworks:** C/C++, Python, Bash; Assembly (x86, ARM, RISC-V); Parallel Programming (Pthreads, OpenMP, MPI); Hardware Description (VHDL, Verilog).
- **Tools & Methodologies:** Architecture Simulators (Gem5, ChampSim, PyMTL); ASIC Synthesis (Synopsys Design Compiler, Yosys); Energy Modeling (CACTI, McPAT); Circuit Design (HSPICE); Version Control (Git); Containerization (Docker, Podman).